## Abstract of the Disclosure

A linked list buffer circuit can be configured to store different linked lists. The buffer includes insert logic and an insert state machine to add ATM cells to the linked lists in the buffer. Extract logic and an extract state machine allow for the removal of ATM cells from the linked lists in the buffer. Because, ATM cells can have different levels of priority, programmable monitor circuitry is provided to monitor the linked lists in the buffer. The monitor circuitry keeps track of buffer and list capacity, and also keeps track of cell loss priority and delay priority cells of the buffer and the linked lists. This information is used to drop received cells if necessary. The linked list monitor circuitry can be configured based upon the linked list configuration of the buffer. The linked list monitor can be configured by changing threshold levels provided to counter/comparator circuitry. Assignments of internal counter circuitry are also programmable based upon the buffer configuration.